Flexible LDPC Decoder IP For NR-5G

V1.1

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Revision History

Date	Version	Revision
2018.08.01	V1.0	Initial release
2018.08.07	V1.1	Co-design with 802.11n/ac LDPC codes decoder

The LDPC Decoder is a highly optimized IP core intended to work with Xilinx FPGAs or ASIC implementation. The LDPC Decoder benefits from a flexible structure to fit almost all Quasi-Cyclic (QC) LDPC codes in arbitrary code length and code rate configuration by passing different parameters and a little modification to Verilog codes.

NR-5G LDPC code is designed very flexible to be used with many code length and code rate configurations, and the maximum parallel size is up to 384. The NR-5G LDPC Decoder IP is made as an example and described below.

Features

- 5G NR LDPC codes decoder support both base graphs and all Zc sizes and code rate configs
- Throughput up to 2.071Gbps @8 iterations @200MHz on Xilinx Virtex UltraScale FPGA VCU095

Overview

The LDPC Decoder benefits from a flexible structure. Custom and standardized LDPC codes are supported through the ability to specify the parity check matrix through modification of H matrix ROM and the barrel shifter module. A block diagram of the LDPC Decoder core is shown in Figure 1.

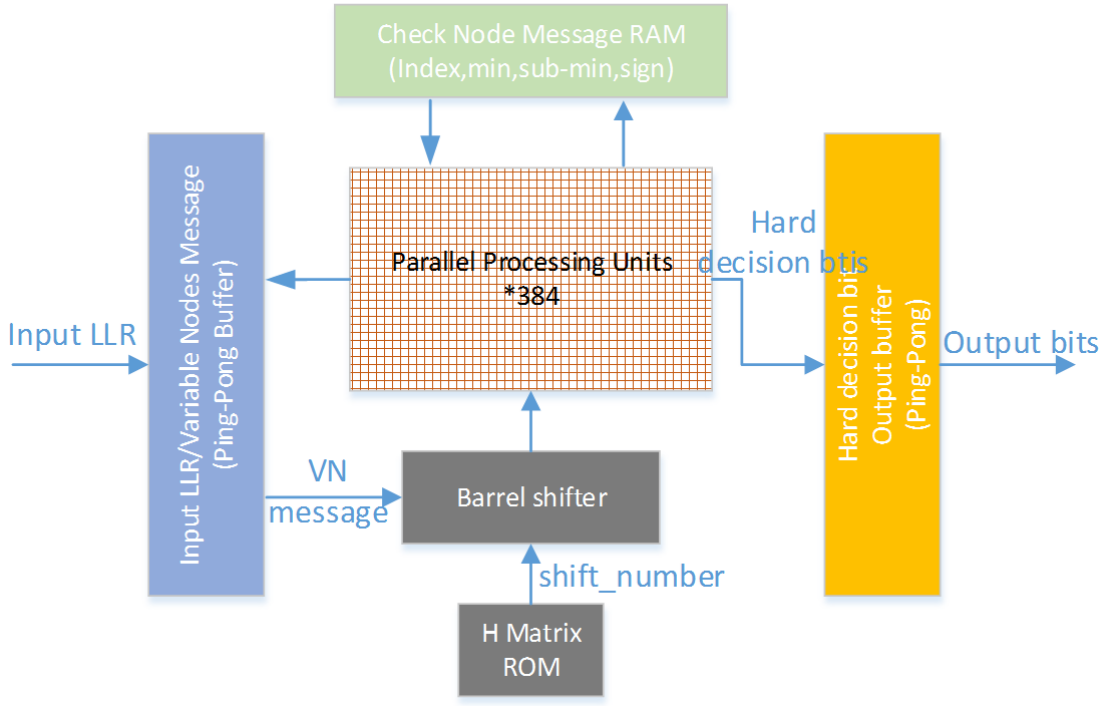

Figure 1: LDPC Decoder Core Block Diagram

Feature Summary

The LDPC Decoder core is a highly flexible soft-decision LDPC decoder with the following features:

- Layered Massage Passing decoding scheme
  Implemented in fixed-point Row-Message-Passing layered decoding algorithm with faster convergence speed.
- Normalize Min-Sum decoding algorithm
  Normalization Factor is 0.75. It's optional to adjust the normalization factor as the iteration cycles on going.
- Highly parallel structure to supply high throughput and low latency performance
  Working on Maximum 384 parallel Units for NR-5G.
- High configurable codes
  A range of quasi-cyclic codes can be supported by modifying the H matrix ROM and barrel shifter modules. For different configuration, data width of input ports/ output ports/ inner wires and registers definition is written in parameter Verilog data-type. Scaling and customizing of the decoder can be achieved easily.
- Flexibility to do on-the-fly running
  When running NR-5G codes (or other standardized codes), different base graph, H matrix selection, Zc size, iteration number can be configured on-the-fly and changed block-by-block.
- Input 6-bit width LLRs are always organized in parallel of 16, if LLR length is not multiples of 16, zeroes padding should be attached to the last input cycle.
- Output Hard-Decision bits are always organized in parallel of 16 too. Also, zeroes padding is attached if necessary.
- Number of iteration 1~64
- Early Stop criteria
  Stop criteria can be configured to be one of the three: a) Parity Check passes; b) Parity Check passes in tow continuous iteration cycles; c) Maximum iteration number is reached.

Resource Utilization

Implemented on Xilinx Virtex UltraScale VCU095. LUT is 6-input, RAM size is 36kbits.

Parallelism	LUT	FF	RAM	DSP48
384	106951	62062	122.5	0

Deliverables

• Verilog RTL source code or synthesized netlist
• Verilog HDL simulation models and testbench with random regression environment for VCS
• Bit-accurate Matlab, C or C++ golden model
• Comprehensive documentation